Low-power Audio Amplifier for Telephone Applications

U4083B

Features

- Wide Operating Voltage Range: 2V to 16V
- Low Current Consumption: 2.7 mA Typically
- Chip Disable Input to Power Down the Integrated Circuit
- Low Power-down Quiescent Current
- Drives a Wide Range of Speaker Loads
- Output Power P_o = 250 mW at R_L = 32Ω (Speaker)
- Low Harmonic Distortion (0.5% Typically)
- Wide Gain Range: 0 dB to 46 dB

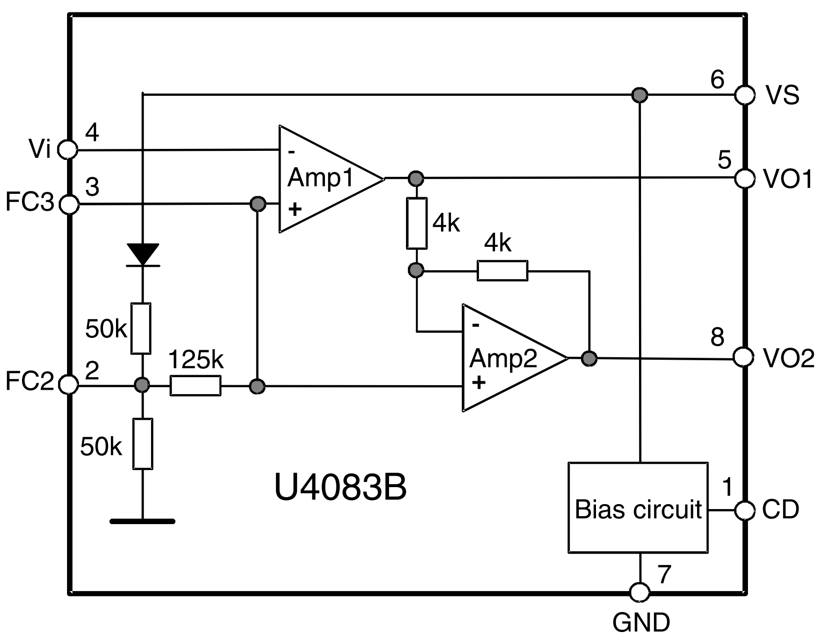
Benefits

- Low Number of External Components
- Low Current Consumption

1. Description

The integrated circuit U4083B is a low-power audio amplifier for telephone loudspeakers. It has differential speaker outputs to maximize the output swing at low supply voltages. There is no need for coupler capacitors. The U4083B has an open-loop gain of 80 dB where the closed-loop gain is adjusted with two external resistors. A chip disable pin permits powering down and/or muting the input signal.

Figure 1-1. Block Diagram



Rev. 4655C–CORD–03/06

2. Pin Configuration

Figure 2-1. Pinning SO8

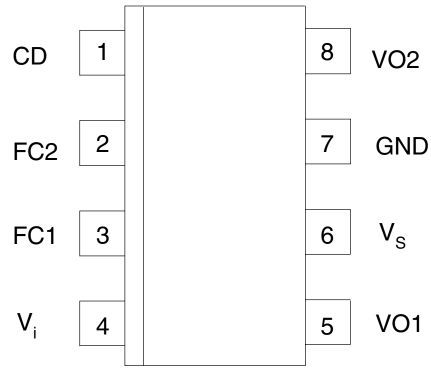


Table 2-1. Pin Description

Pin	Symbol	Function
1	CD	Chip disable
2	FC2	Filtering, power supply rejection
3	FC1	Filtering, power supply rejection
4	V_i	Amplifier input
5	VO1	Amplifier output 1
6	V_S	Voltage supply
7	GND	Ground
8	VO2	Amplifier output 2

3. Functional Description Including External Circuitry

3.1 Pin 1: Chip Disable Digital Input (CD)

Pin 1 (chip disable) is used to power down the IC to conserve power or mute the IC or both.

Input impedance at Pin 1 is typically 90 kΩ.

- Logic 0 < 0.8V IC enabled (normal operation)
- Logic 1 > 2V IC disabled

Figure 8-15 on page 12 shows the power supply current diagram. The change in differential gain from normal operation to muted operation (muting) is more than 70 dB.

Switching characteristics are as follows:

- Turn-on time t_{on} = 12 ms to 15 ms
- Turn-off time $t_{off} \leq 2$ µs

They are independent of C_1, C_2 and V_S.

Voltages at Pins 2 and 3 are supplied from V_S and, therefore, do not change when the U4083B is disabled. The outputs, V_{O1} (Pin 5) and V_{O2} (Pin 8), turn to a high impedance condition by removing the signal from the speaker.

When signals are applied from an external source to the outputs (disabled), they must not exceed the range between the supply voltage, V_S, and ground.

3.2 Pins 2 and 3: Filtering, Power Supply Rejection

Power supply rejection is provided by capacitors C_1 and C_2 at Pin 3 and Pin 2, respectively. C_1 is dominant at high frequencies whereas C_2 is dominant at low frequencies (Figure 8-4 on page 8 to Figure 8-7 on page 9). The values of C_1 and C_2 depend on the conditions of each application. For example, a line-powered speakerphone (telephone amplifier) will require more filtering than a system powered by regulated power supply.

The amount of rejection is a function of the capacitors and the equivalent impedance at Pin 3 and Pin 2 (see electrical characteristic equivalent resistance, R).

Apart from filtering, capacitors C_1 and C_2 also influence the turn-on time of the circuit at power up, since the capacitors are charged up through the internal resistors (50 kΩ and 125 kΩ) as shown in the block diagram.

Figure 8-1 on page 7 shows the turn-on time versus C_2 at V_S = 6V, for two different C_1 values.

The turn-on time is 60% longer when V_S = 3V and 20% shorter when V_S = 9V.

The turn-off time is less than 10 µs.

3.3 Pin 4: Amplifier Input V_i, Pin 5: Amplifier Output 1 V_{O1}, Pin 8: Amplifier Output 2 V_{O2}

There are two identical operational amplifiers. Amplifier 1 has an open-loop gain ≥ 80 dB at 100Hz (Figure 8-2 on page 7), whereas the closed-loop gain is set by external resistors, R_f and R_i (Figure 8-3 on page 8). The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. A closed-loop gain of 46 dB is recommended for a frequency range of 300Hz to 3400Hz (voice band). Amplifier 2 is internally set to a gain of –1.0 dB (0 dB). The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. Output voltage swing is between 0.4V and V_S – 1.3V at maximum current (Figure 8-18 on page 13 and Figure 8-19 on page 13).

The output DC offset voltage between Pins 5 and 8 ($V_{O1} - V_{O2}$) is mainly a function of the feedback resistor, R_f, because the input offset voltages of the two amplifiers neutralize each other.

Bias current of Amplifier 1 which is constant with respect to V_s, flows out of Pin 4 (V_i) and through R_f, forcing V_{O1} to shift negative by an amount equal to $R_f I_{IB}$ and V_{O2} positive to an equal amount.

The output offset voltage specified in the electrical characteristics is measured with the feedback resistor (R_f = 75 kΩ) shown in the typical application circuit, Figure 8-20 on page 14. It takes into account the bias current as well as internal offset voltages of the amplifiers.

3.4 Pin 6: Supply and Power Dissipation

Power dissipation is shown in Figure 8-8 on page 9 to Figure 8-10 on page 10 for different loads. Distortion characteristics are given in Figure 8-11 on page 10 to Figure 8-13 on page 11.

$$P_{totmax} = \frac{T_{jmax} - T_{amb}}{R_{thJA}}$$

where

T_{jmax} = Junction temperature = 140°C

T_{amb} = Ambient temperature

R_{thJA} = Thermal resistance, junction-ambient

Power dissipated within the IC in a given application is found from the following equation:

$P_{tot} = (V_S \times I_S) + (I_{RMS} \times V_S) - (R_L \times I_{RMS}^2)$

I_S is obtained from Figure 8-15 on page 12.

I_{RMS} is the RMS current at the load R_L.

The IC's operating range is defined by a peak operating load current of ±200 mA (Figure 8-8 on page 9 to Figure 8-13 on page 11). It is further specified with respect to different loads (see Figure 8-14 on page 12). The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the integrated circuit. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above mentioned equation.

3.5 Layout Considerations

Normally, a snubber is not needed at the output of the IC, unlike many other audio amplifiers. However, the PC-board layout, stray capacitances, and the manner in which the speaker wires are configured may dictate otherwise. Generally, the speaker wires should be twisted tightly, and should not be more than a few cm (or inches) in length.

4. Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Reference point pin 7, T_{amb} = 25° C unless otherwise specified.

Parameters		Symbol	Value	Unit
Supply voltage	Pin 6	V_S	–1.0 to +18	V
Voltages Disabled	Pins 1, 2, 3 and 4 Pins 5 and 8		–1.0 to (V_S + 1.0) –1.0 to (V_S + 1.0)	V V
Output current	Pins 5 and 8		±250	mA
Junction temperature		T_j	+140	°C
Storage temperature range		T_{stg}	–55 to +150	°C
Ambient temperature range		T_{amb}	–20 to +70	°C
Power dissipation SO8: T_{amb} = 60°C		P_{tot}	440	mW

5. Thermal Resistance

Parameters		Symbol	Value	Unit
Junction ambient	SO8	R_{thJA}	180	K/W

6. Recommended Operating Conditions

Parameters		Symbol	Value	Unit
Supply voltage	Pin 6	V_S	2 to 16	V
Load impedance	Pins 5 to 8	R_L	8.0 to 100	Ω
Load current		I_L	±200	mA
Differential gain (5.0 kHz bandwidth)		DG	0 to 46	dB
Voltage at CD	Pin 1	V_{CD}	V_S	V
Ambient temperature range		T_{amb}	–20 to +70	°C

7. Electrical Characteristics

T_{amb} = +25°C, reference point pin 7, unless otherwise specified

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Amplifiers (AC Characteristics)						
Open-loop gain (Amplifier 1, f < 100Hz)		G_{VOL1}	80			dB
Closed-loop gain (Amplifier 2)	V_S = 6.0V, f = 1.0 kHz, R_L = 32Ω	G_{V2}	–0.35	0	+0.35	dB
Gain bandwidth product		G_{BW}		1.5		MHz
Output power	V_S = 3.0V, R_L = 16Ω, d < 10% V_S = 6.0V, R_L = 32Ω, d < 10% V_S = 12V, R_L = 100Ω, d < 10%	P_O P_O P_O	55 250 400			mW
Total harmonic distortion (f = 1.0 kHz)	V_S = 6.0V, R_L = 32Ω, P_o = 125 mW V_S > 3.0V, R_L = 8Ω, P_o = 20 mW V_S > 12V, R_L = 32Ω, P_o = 200 mW	d d d		0.5 0.5 0.6	1.0	%
Power supply rejection ratio	V_S = 6.0V, ΔV_S = 3.0V C_1 = α, C_2 = 0.01 µF C_1 = 0.1 µF, C_2 = 0, f = 1.0 kHz C_1 = 1.0 µF, C_2 = 5.0 µF, f = 1.0 kHz	PSRR PSRR PSRR	50	12 52		dB
Muting	V_S = 6.0V, 1.0 kHz < f < 20 kHz, CD = 2.0V	G_{MUTE}		>70		dB
Amplifiers (DC Characteristics)						
Output DC level at V_{O1}, V_{O2} R_f = 75 kW	V_S = 3.0V, R_L = 16Ω V_S = 6.0V V_S = 12V	V_O V_O V_O	1.0	1.15 2.65 5.65	1.25	V
Output high level	I_O = –75 mA, 2.0V < V_S < 16V	V_{OH}		V_S – 1		V
Output low level	I_O = –75 mA, 2.0V < V_S < 16V	V_{OL}		0.16		V
Output DC offset voltage (V_{O1} – V_{O2})	V_S = 6.0V, R_f = 75 kΩ, R_L = 32Ω	ΔV_O	–30	0	+30	mV
Input bias current at V_i	V_S = 6.0V	$-I_{IB}$		100	200	nA
Equivalent resistance at Pin 3	V_S = 6.0V	R	100	150	220	kΩ
Equivalent resistance at Pin 2	V_S = 6.0V	R	18	25	40	kΩ
Chip disable Pin 1 Input voltage low Input voltage high Input resistance	V_S = V_{CD} = 16V	V_{IL} V_{IH} R_{CD}	2.0 50	90	0.8 175	V V kΩ
Power supply current	V_S = 3.0V, R_L = α, CD = 0.8V V_S = 16V, R_L = α, CD = 0.8V V_S = 3.0V, R_L = α, CD = 2.0V	I_S I_S I_S		65	4.0 5.0 100	mA mA µA

8. Typical Temperature Performance

T_{amb} = –20 to +70° C

Function	Typical Change	Units
Input bias current at V_i	±40	pA/° C
Total harmonic distortion V_S = 6.0V, R_L = 32 Ω, P_o = 125 mW, f = 1.0 kHz	+0.003	%/° C
Power supply current V_S = 3.0V, R_L = α, CD = 0V V_S = 3.0V, R_L = α, CD = 2.0V	–2.5 –0.03	µA/° C µA/° C

Figure 8-1. Turn-on Time versus C_1 and C_2 at Power On

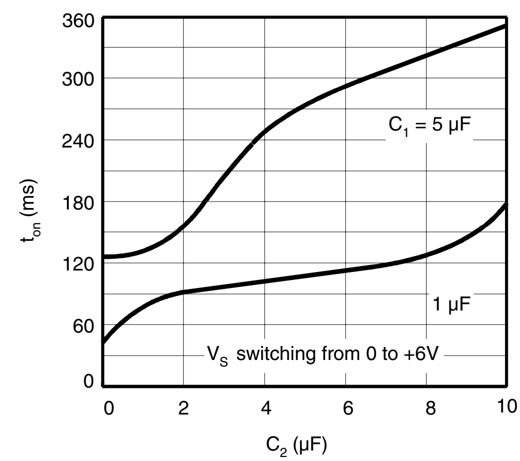


Figure 8-2. Amplifier 1 — Open-loop Gain and Phase

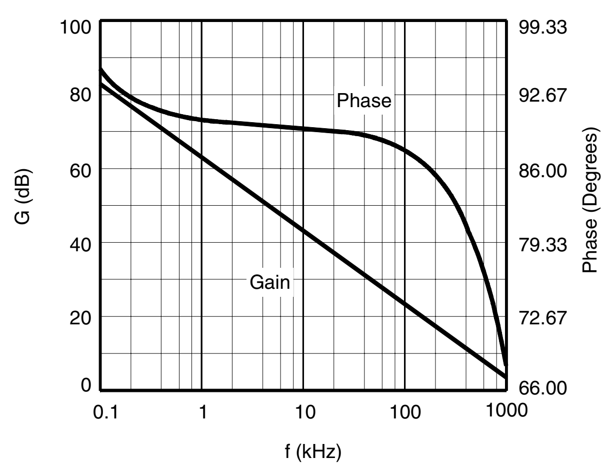


Figure 8-3. Differential Gain versus Frequency

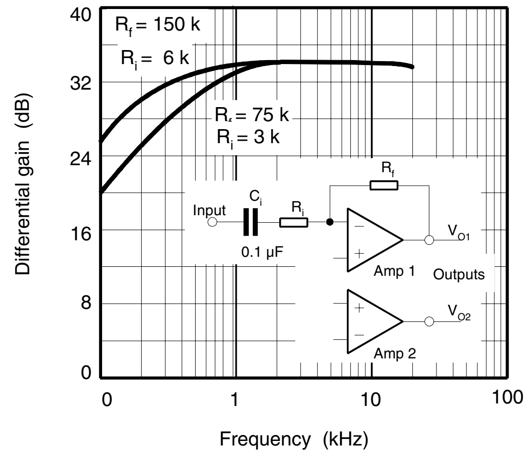


Figure 8-4. Power Supply Rejection versus Frequency — C_2 = 10 µF

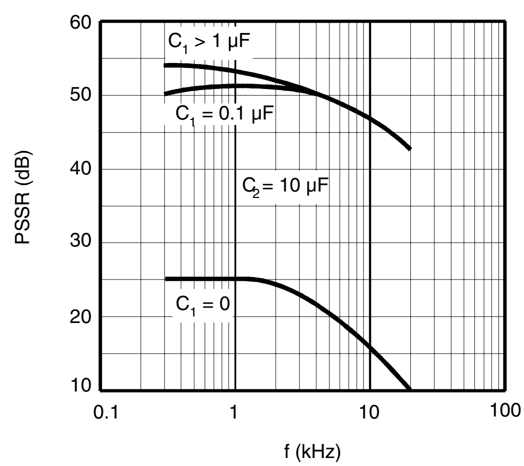


Figure 8-5. Power Supply Rejection versus Frequency — C_2 = 5 µF

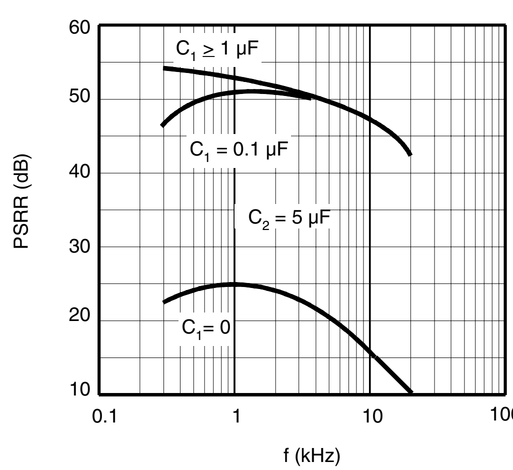


Figure 8-6. Power Supply Rejection versus Frequency — C_2 = 1 µF

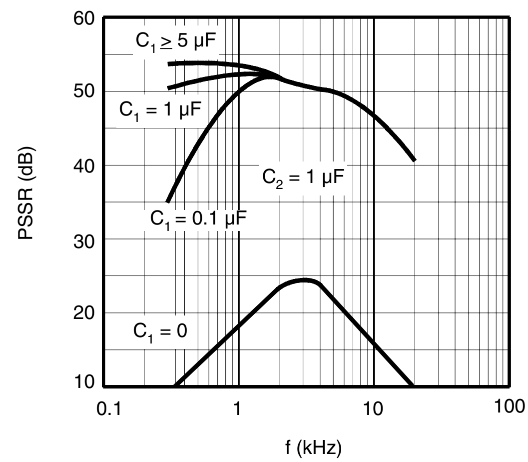


Figure 8-7. Power Supply Rejection versus Frequency — C_2 = 0

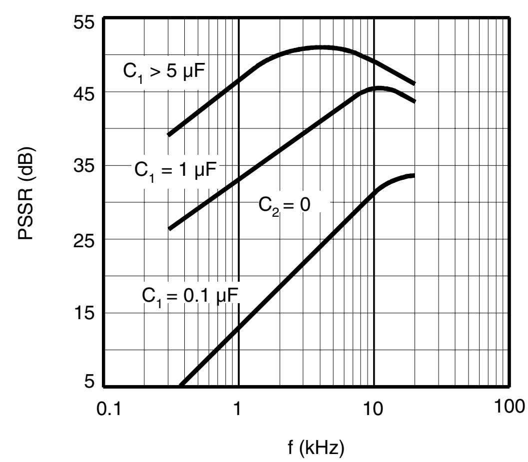


Figure 8-8. Device Dissipation — R_L = 8Ω

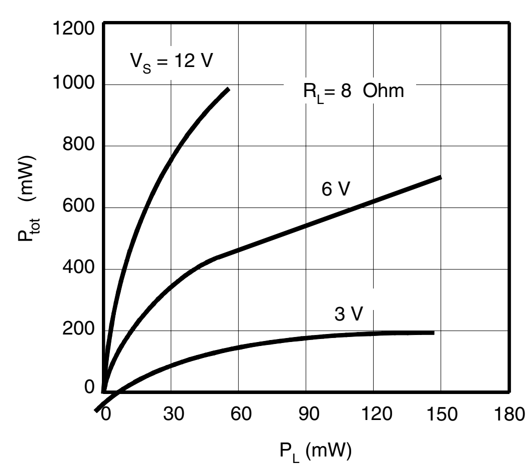


Figure 8-9. Device Dissipation — R_L = 16Ω

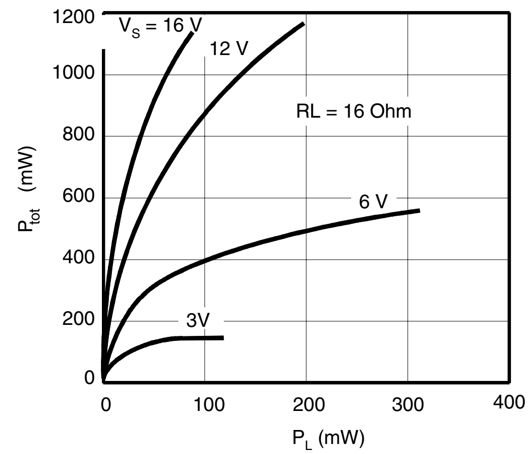


Figure 8-10. Device Dissipation — R_L = 32Ω

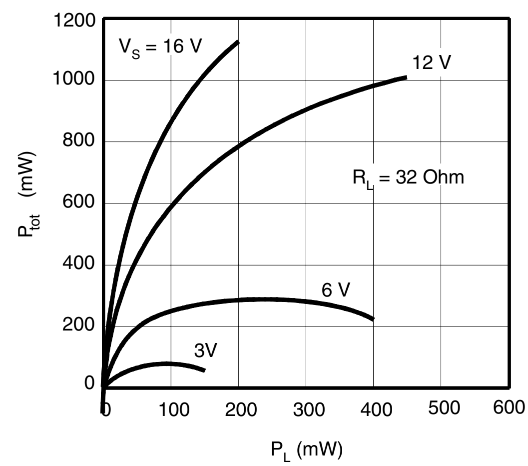


Figure 8-11. Distortion versus Power — f = 1 kHz, Delta – G_V = 34 dB

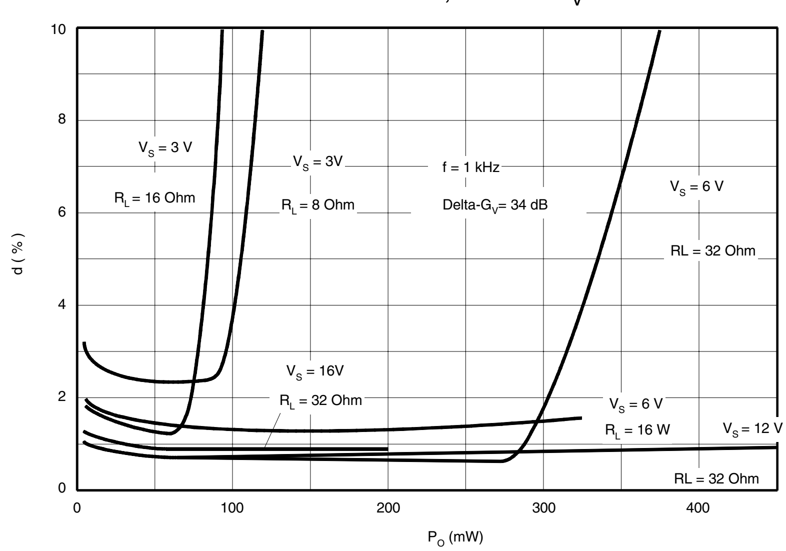


Figure 8-12. Distortion versus Power — f = 3 kHz, Delta – G_V = 34 dB

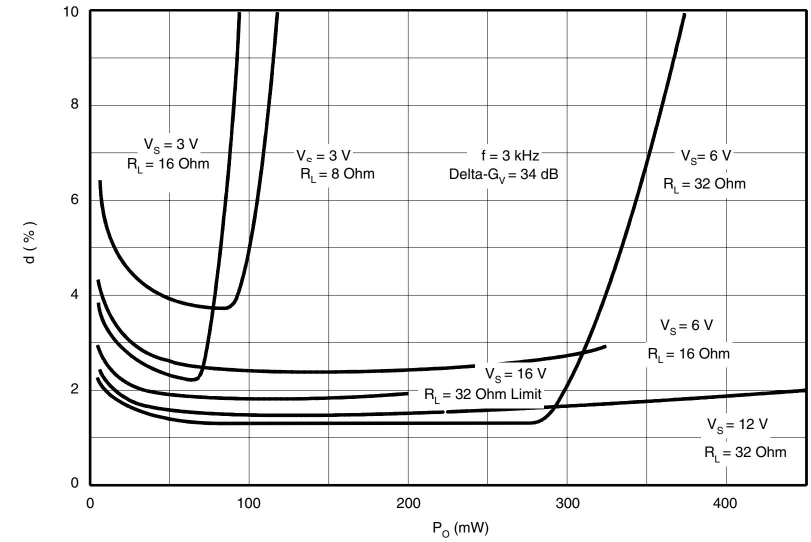


Figure 8-13. Distortion versus Power — f = 1 kHz or 3 kHz, Delta – G_V = 12 dB

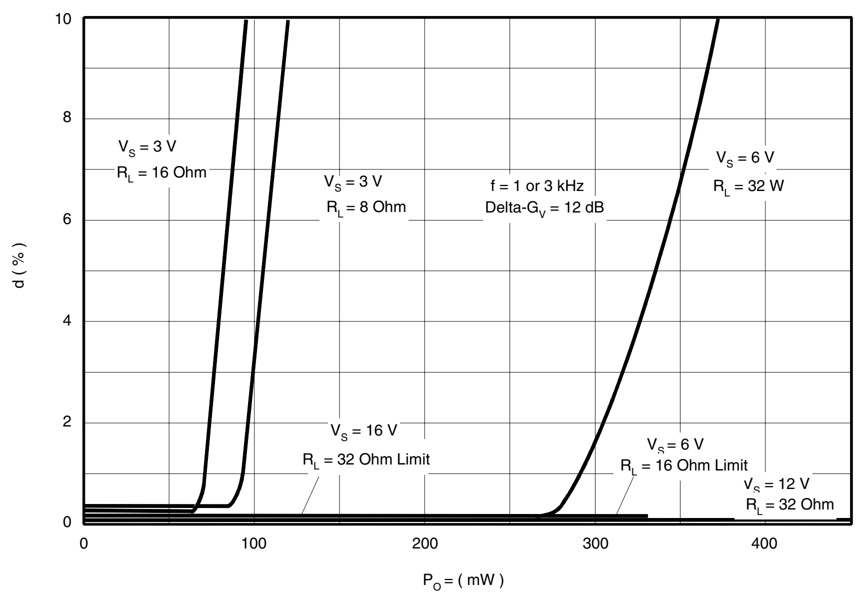


Figure 8-14. Maximum Allowable Load Power

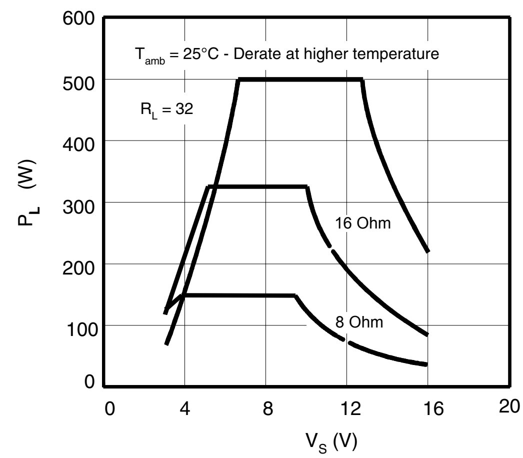


Figure 8-15. Power-supply Current

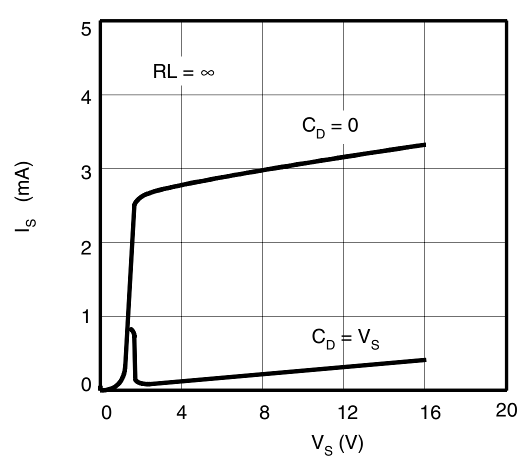


Figure 8-16. Small Signal Response

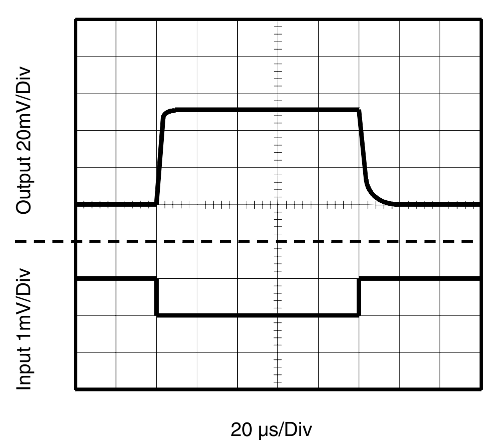


Figure 8-17. Large Signal Response

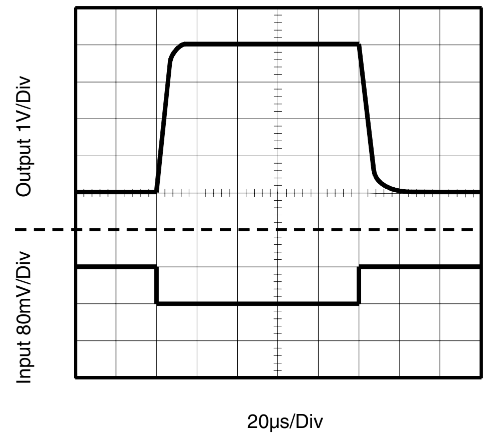


Figure 8-18. V_S – V_{OH} versus Load Current

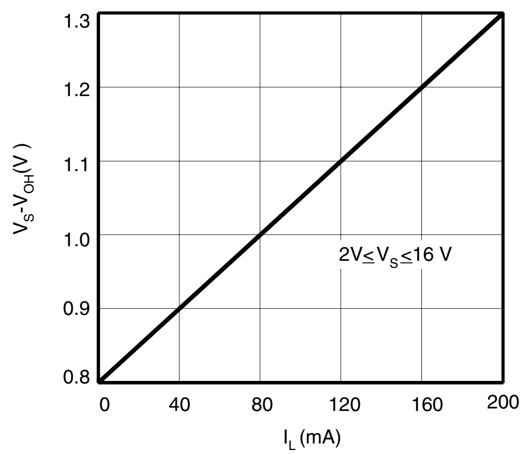


Figure 8-19. V_{OL} versus Load Current

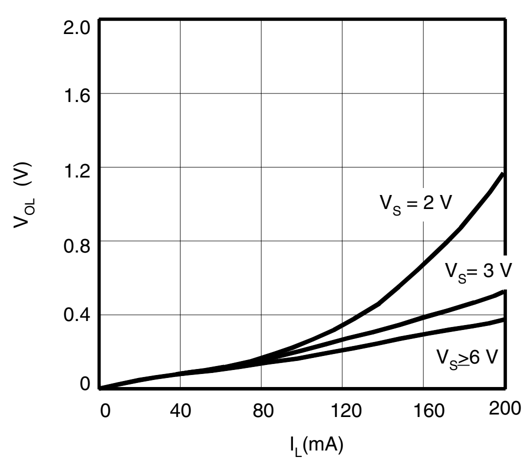
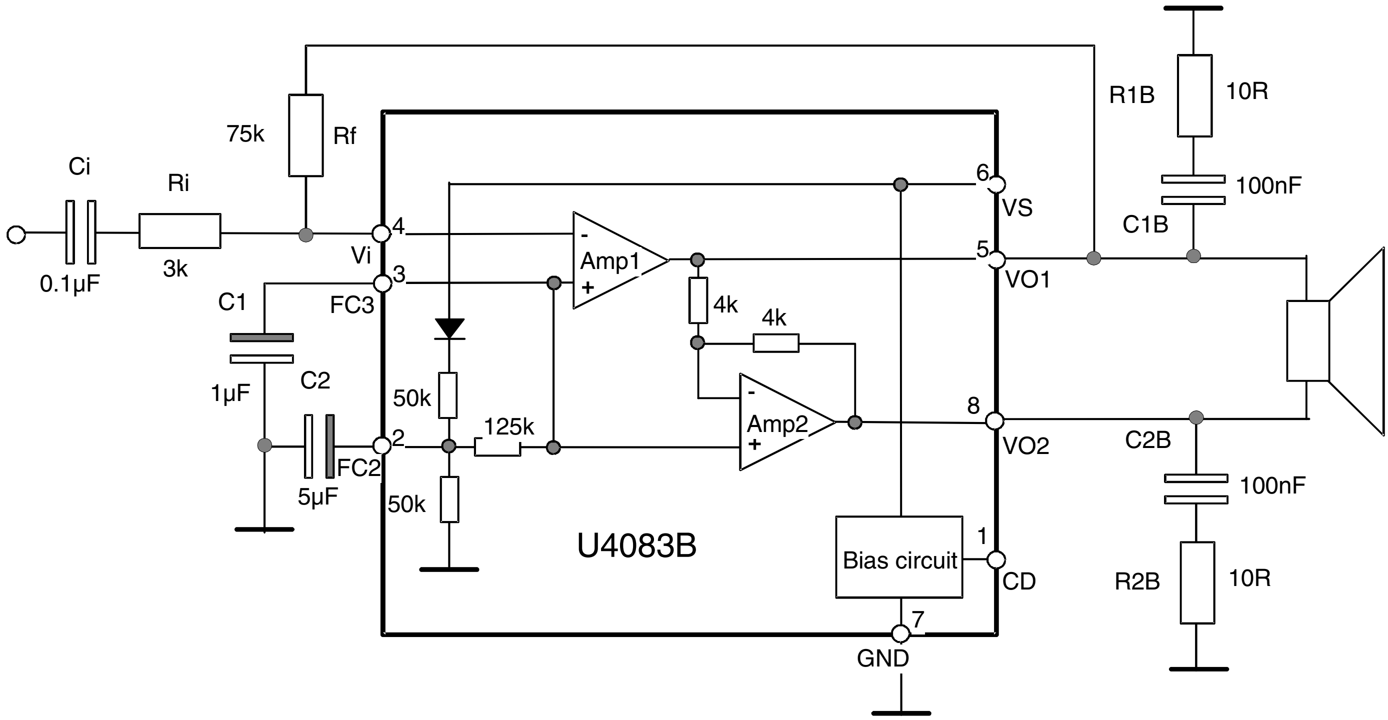


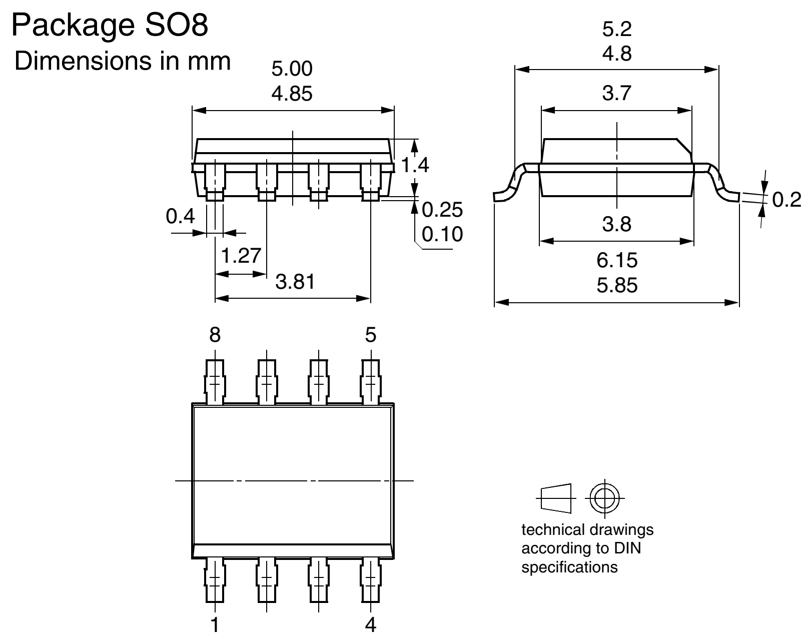
Figure 8-20. Application Circuit



9. Ordering Information

Extended Type Number	Package	Remarks
U4083B-MFPY	SO8, Pb-free	Tube
U4083B-MFPG3Y	SO8, Pb-free	Taped and reeled

10. Package Information



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
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Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
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Maxwell Building
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Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

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Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
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